Pre-Programming e.MMC Devices before SMT Reflow

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Associated Part Family:S40FCxxx

1 Introduction

This application note AN200005 provides information on the requirement of pre-programming in pSLC mode before SMT reflow process for SkyHigh e.MMC memory device.

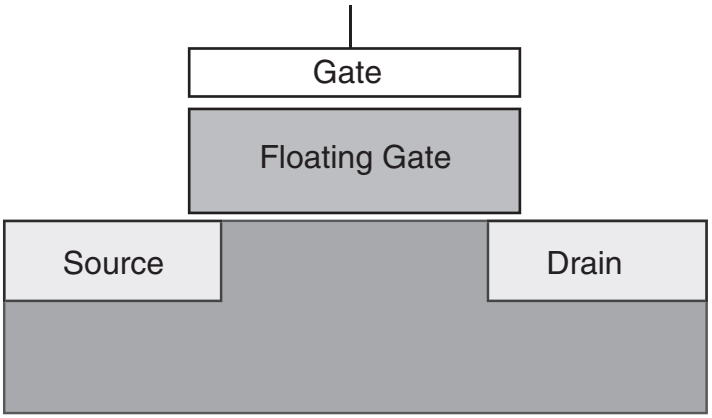
This document applies to the following SkyHigh devices:

- S40FCxxx e.MMC series

SLC Versus MLC NAND Flash Memory

2 NAND Flash Overview

A flash memory cell consists of a single transistor with a floating gate that can store electrons. The number of electrons on the floating gate can alter the threshold voltage (V_t) of the transistor and this is what determines if the cell is programmed '0' or erased '1'.



SLC flash memory is where a single physical cell can store one bit of data. It can have two states, '0' (programmed) or '1' (erased).

Figure 1. Floating Gate Flash Transistor Cross-Section

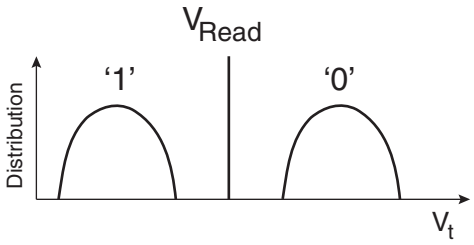


Figure 2. SLC V_t Distribution

SLC Versus MLC NAND Flash Memory

MLC flash memory is where a single physical cell can store two bits of data. It can have four states, ‘00’ (programmed), ‘01’ (partially programmed), ‘10’ (partially erased), or ‘11’ (erased). Programming for an MLC device needs to be carefully done so that the V_t is within the window for the desired state.

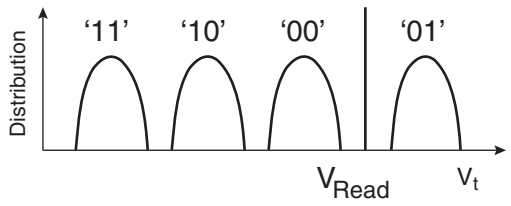


Figure 3. MLC V_t Distribution

3 SLC vs MLC Specification Comparison

Table 1 is a comparison of key specifications between SLC and MLC NAND flash memory.

Table 1. Feature Comparison between SLC and MLC Devices.

Features	SLC	MLC
Bits per Cell	1	2
Voltage	3.3V, 1.8V	3.3V
Data Bus Width (Bits)	x8, x16	x8
Planes	1 or 2	2 or more
Page Size (Bytes)	2k	4k or more
Pages Per Block	64	128 or more
ECC (per 512 Bytes)	4-bit or more	12-bit or more
Program/Erase Cycles	100k	3k to 5k
Number of Partial Pages	4	1
Read	25 µs	50 to 60 µs
Program	200 µs	1100 to 1300 µs
Erase	2 ms	3 to 4 ms

Note:

1. *Based off of 3X and 2X technology nodes.*

Since MLC contains two bits of data per cell versus one bit of data per cell for SLC, it is easy to see that MLC has a distinct advantage in offering higher density products. Assuming the wafer size and process technology are the same, a MLC product will have about 2X the density of the SLC product.

SLC has a clear advantage in most other areas such as write performance, endurance, and lower error rates. Write performance is worse on the MLC device since it requires a more extensive programming algorithm. The algorithm needs to carefully store charge on the floating gate to get the V_t's within a tight window for the desired programming state.

SLC will have 10x better endurance as compared to a MLC device. Programming the flash cell can lead to damage in the oxide layer which could alter the V_t of the cell. This is true for both a SLC and MLC device. However, a MLC device has a much tighter window for the V_t placement, so any damage to the oxide layer will be felt earlier on the MLC device than the SLC device. Consequently, a SLC device is rated at a minimum of 100,000 program/erase cycle and a MLC device is rated at a minimum of 3,000 program/erase cycles.

SLC will have a lower Raw Bit Error Rate (RBER) than a MLC device. Leakage or disturbs could shift the V_t within the cell and lead to a read error. Due to the tight window of Vt placement for a MLC device, it is more susceptible to a read error. With a higher error rate for the MLC device, it will require a stronger ECC (Error Code Correction) to protect against read errors. The processor or controller will need to support the larger ECC algorithms. SLC would be a better choice for older processors which only support smaller ECC algorithms.

4 Pre Programming Data Before SMT Reflow

Data retention is the ability of flash to maintain data integrity of stored data over time. As process geometries shrink down to sub 20nm, data retention through the SMT reflow becomes more challenging for MLC flash devices. Compared with the single-level cell flash memory, the multi-level cell flash memory is much more susceptible to data corruption and data loss. The charge loss is strongly impacted by the temperature, P/E cycling, and the type of flash used (SLC, MLC). In SLC flash, the cells are programmed to a level near the maximum Vt, giving the flash a very large margin for charge loss before a bit error occurs as illustrated in figure 4. However, MLC flash uses the same margin area to create four data regions, significantly reducing the margin for charge loss and bit errors as shown in Figure 5.
Therefore, During the SMT reflow process, data pre-programmed in a multi-level cell flash memory is more exposed to data Loss due to high temperature process, thus causing data corruption of the pre-programmed data.
After high temperature SMT reflow processing, cell NAND threshold voltages for MLC NAND can shift beyond the reference voltage due to charge leakage, causing data retention read errors. Retention errors, caused by charge leakage over time, are the dominant source of flash memory errors.

SkyHigh Memory e.MMC devices can be configured in either MLC mode or pSLC mode as specified by JEDEC e.MMC specifications. The Pseudo-SLC (pSLC) storage devices store only one bit per cell like SLC flash. The flash controller treats the erased state as 1 and any programmed state as 0. Using the MLC flash in pSLC mode improves the margin against charge loss and bit errors.
SkyHigh Memory requires any e.MMC pre-programmed data prior to high temperature SMT Reflow to be performed in pSLC mode

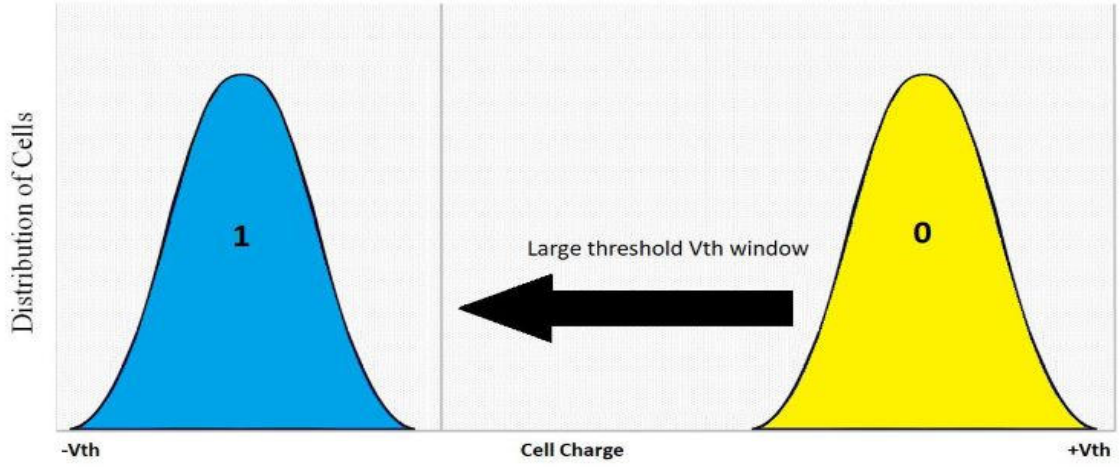


Figure 4. SLC V_t Distribution

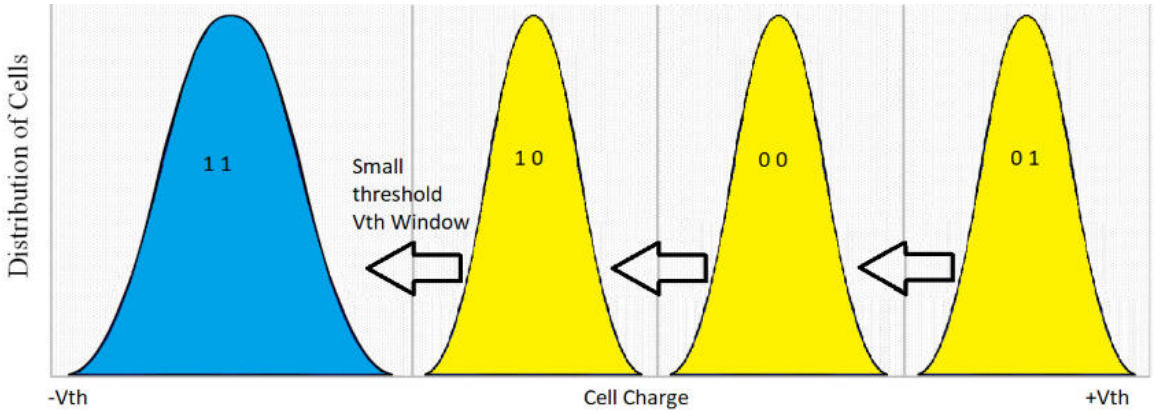


Figure 5. MLC V_t Distribution

5 Reflow Conditions

e.MMC parts are qualified per the reflow profile attached below, unless otherwise specified. The specifics of the of the reflow profile are also attached, and are obtained from J-STD-020.

Table 2
Reflow Profiles (per Jedec J-STD-020D.1)

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Ramp-up rate (TL to Tp)	3 °C/second max.	3 °C/second max.
Liquidous temperature (TL) Time (tL) maintained above TL	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body temperature (Tp)	For users Tp must not exceed the Classification temp in Table 2A. For suppliers Tp must equal or exceed the Classification temp in Table 2A	For users Tp must not exceed the Classification temp in Table 2B. For suppliers Tp must equal or exceed the Classification temp in Table 2B
Time (tp)* within 5 °C of the specified classification temperature (Tc), see Table 2a & 2B Figure 5-1. J-STD-020D.1	20* seconds	30* seconds
Ramp-down rate (Tp to TL)	6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum .		

Table 2A
SnPb Eutectic Process - Classification Temperatures (Tc)

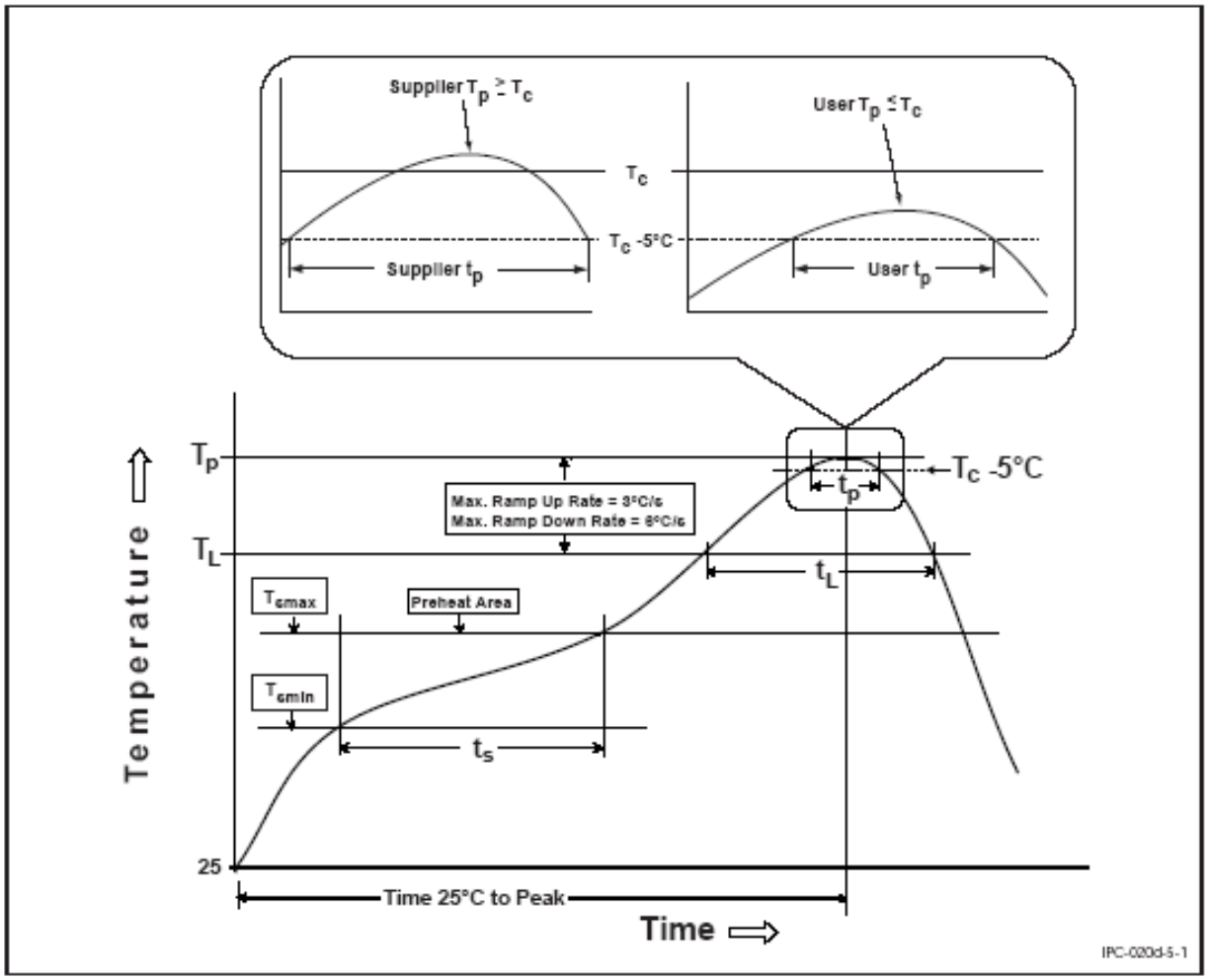
Package Thickness	Volume mm3 <350	Volume mm3 >=350
<2.5 mm	235 °C	220 °C
>=2.5 mm	220 °C	220 °C

Table 2B
Pb-Free Process -Classification Temperatures (Tc)

Package Thickness	Volume mm3 <350	Volume mm3 350 - 2000	Volume mm3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	260 °C	245 °C	245 °C

Note:
1. The use of a higher Tp does not change the classification temperature (Tc).
2. All temperatures refer to topside of the package, measured on the package body surface.
3. Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or nonintegral heat sinks.
4. Moisture sensitivity levels of components intended for use in a Pb-free assembly process shall be evaluated using the Pb-free classification temperatures and profiles defined in Tables 2 and 2B, whether or not Pb-free.

Appendix A
Solder Reflow Temperature Profile



Classification Profile (Not to scale)

6 Conclusion

This application note provides information about Pre-Programming SkyHigh Memory before high temperature SMT reflow for e.MMC memory devices. After high temperature processing, Multi-level cell NAND threshold voltages can shift beyond the reference voltage, causing read errors and potential data corruption. In order to guarantee long term reliability, SkyHigh Memory requires any pre-programming to e.MMC devices prior to the SMT reflow to be performed in pSLC mode. The device can be used in either pSLC or MLC modes after the SMT reflow process is completed.

Please contact factory for pre-programming prior to the SMT reflow process.

7 Document History Page

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Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	–	06/13/2022	Initial version